IN THE CLAIMS:
1-27. (Canceled)

28. (Currently amended) A semiconductor device, comprising:

a first interlayer insulating layer;

a plurality of wiring lines which are formed of copper (Cu), said plurality of wiring lines formed on said first interlayer insulating layer, at least two of said wiring lines being separated from each other by at least a distance predetermined to approach a value, approximately 0.2 to 0.3 μm, for which atoms of said Cu will be unlikely to diffuse through an insulator between said wiring lines in a quantity sufficient to allow a breakdown in an electrical insulation between said wiring lines;

~~an~~ a first insulating layer which has a property that Cu atoms diffuse into said insulating layer in accordance with a diffusion gradient but is unlikely to enter said insulating layer beyond said predetermined distance, ~~and~~ which said predetermined distance thereby effectively insulates between said plurality of wiring lines; and

a second interlayer insulating layer formed on said first insulating layer having the property that the Cu is unlikely to enter therein,

wherein said diffusion gradient of said first insulating layer has a surface region whose Cu concentration is equal to or higher than 10^{19} atoms/cm^3 and approaches no more than an order of magnitude of 10^{18} atoms/cm^3 within one-half of said predetermined distance.

29. (Currently amended) The semiconductor device according to claim 28, wherein said insulating layer has an inner region whose Cu concentration is lower than 10^{19} atoms/cm^3, in

acccordance with said diffusion gradient.

30. (Previously presented) The semiconductor device according to claim 29, wherein said insulating layer comprises Hydrogen Silsesquioxane (HSQ).

31. (Previously presented) The semiconductor device according to claim 30, wherein a thickness of said insulating layer comprising HSQ is equal to or more than 50 nm.

32. (Currently amended) A semiconductor device, comprising:

a plurality of copper (Cu) wiring lines; and

an insulating layer which insulates between said plurality of Cu wiring lines, wherein:

said insulating layer has a surface region respectively adjacent to said wiring lines whose Cu concentration is equal to or higher than 10^{19} atoms/cm^3 due to a diffusion of Cu from said Cu wiring lines, said concentration decreasing radially outward from said surface region in an inner region in accordance with a diffusion gradient to between 10^{19} and 10^{18} atoms/cm^3, and

a separation distance between at least two of said Cu wiring lines approaches a minimum consistent with maintaining a ~~separation between said surface regions~~ region therebetween that has a concentration of said diffused Cu that is no greater than an order of magnitude of 10^{18} atoms/cm^3.

33. (Canceled)

34. (Currently amended) The semiconductor device according to claim ~~33~~ 32 , wherein said insulating layer comprises Hydrogen Silsesquioxane (HSQ).

35. (Previously presented) The semiconductor device according to claim 34, wherein a thickness of said insulating layer comprising HSQ is equal to or more than approximately 50 nm.

36. (Previously presented) The semiconductor device according to claim 35, wherein said inner region of said insulating layer is an inner region of a position which is 50 nm or more from a surface of said insulating layer.

37. (Previously presented) The semiconductor device according to claim 36, wherein said insulating layer directly contacts Cu.

38. (Previously presented) A semiconductor device, comprising:

a plurality of copper (Cu) wiring lines; and

an insulating layer which insulates between said plurality of Cu wiring lines, wherein:

said insulating layer has a surface region whose Cu concentration is equal to or higher than 10^{19} atoms/cm^3,

said insulating layer comprises a multi-layer insulating layer which comprises a middle layer comprised of PAE (Poly Arylene Ether) and an upper insulating layer and a lower insulating layer between which said middle layer is sandwiched, said upper and lower

insulating layers each being comprised of HSQ (Hydrogen Silsesquioxane),

openings are formed in predetermined positions in said PAE layer and said HSQ layers, and one of said plurality of said Cu wiring lines is respectively formed in one of said openings,

and

said Cu wiring lines comprise Cu having a concentration equal to or higher than 10^{19} atoms/cm^3, said upper insulating layer and said lower insulating layer thereby forming an insulating layer which has a property that Cu is unlikely to enter said upper and lower insulating layers.

39. (Previously presented) The semiconductor device according to claim 32, further comprising:

a first interlayer insulating layer formed below said insulating layer; and

a second interlayer insulating layer formed on said insulating layer,

wherein said first and second interlayer insulating layers have a property in strength that offsets a property in strength of said insulating layer.

40. (Previously presented) The semiconductor device according to claim 39, wherein said first and second interlayer insulating layers each comprise SiN, and said insulating layer comprises HSQ (Hydrogen Silsesquioxane).

41. (Previously presented) The semiconductor device according to claim 40, further comprising:

a bottom layer formed below said first interlayer insulating layer, said bottom layer having at least one copper conductor line, wherein said first interlayer insulating layer has a hole formed therein, said hole allowing at least one copper conductor line in said bottom layer to connect with one of said plurality of said copper wiring lines.

42. (Previously presented) The semiconductor device according to claim 41, further comprising:

a layer of adhesive material formed at an interface between said insulating layer and each of said plurality of copper wiring lines.

43. (Previously presented) The semiconductor device according to claim 42, wherein said adhesive material comprises tungsten (W).

44. (Previously presented) The semiconductor device of claim 39, further comprising:

a third interlayer insulating layer formed on said insulating layer;

another insulating layer formed on said third interlayer insulating layer, said another insulating layer having a property that Cu is unlikely to enter said another insulting layer;

a second plurality of copper wiring lines formed in said another insulating layer; and

a fourth interlayer insulating layer formed on said another insulating layer.

45. (Previously presented) The semiconductor device according to claim 40, wherein said third and fourth interlayer insulating layers each comprise SiN, and said another insulating layer comprises HSQ (Hydrogen Silsesquioxane).

46. (Previously presented) The semiconductor device according to claim 44, further comprising:

a layer of adhesive material formed at an interface between said another insulating layer and each of said second plurality of copper wiring lines.

47. (Previously presented) The semiconductor device according to claim 46, wherein said adhesive material comprises tungsten (W).

48. (Previously presented) The semiconductor device according to claim 44, wherein said third interlayer insulating layer has a hole formed therein, said hole allowing at least one of said copper wiring lines in said insulating layer to connect with one of said second plurality of said copper wiring lines.

49. (Previously presented) The semiconductor device according to clam 32, wherein:

said insulating layer comprises a first interlayer insulating layer, a middle insulating layer, and a second insulating layer,

said first interlayer insulating layer comprises a first material,

said middle insulating layer is formed on said first interlayer insulating layer and comprises an organic polymer,

said second insulating layer is formed on said middle insulating layer and comprises said first material, and

said first interlayer insulating layer, said middle insulating layer, and said second insulating layer form a system that serves to confine a migration of copper ions from said copper wiring lines to be within said middle insulating layer.

50. (Previously presented) The semiconductor device of claim 49, wherein said first material comprises SiN, and said middle insulating layer comprises hydrogen silsesquioxane (HSQ), said HSQ having a property that a migration of copper ions is limited therein.

51. (Previously presented) The semiconductor device of claim 49, wherein said first material comprises hydrogen silsesquioxane (HSQ) and said middle insulating layer comprises Poly Arylene Ether (PAE), said HSQ having a property that a migration of copper ions is limited therein, so that said first interlayer insulating layer thereby provides a lower layer to confine said migration of copper ions and said second interlayer insulating layer thereby provides an upper layer to confine said migration of copper ions.

52. (Withdrawn) A method of providing a minimal isolation thickness for a copper conductor in an integrated circuit, said method comprising:

providing, for said copper conductor, a predetermined isolation thickness of a low permittivity insulating layer to comprise a high-concentration diffusion region of copper diffusing from said copper conductor, said high-concentration being approximately 10^{19} atoms/cm^3, said predetermined isolation thickness based on a distance that copper diffuses from said copper conductor into said low permittivity insulating layer to a lower

concentration of copper at which a leakage current becomes less significant in said low permittivity insulating layer, said lower concentration being 10^{18} atoms/cm^3 or less, said copper conductor and said low permittivity insulating layer having no barrier layer interposed therebetween,

wherein said high-concentration diffusion region is located such as to be separated from any other similar high-concentration diffusion regions and copper conductors, said predetermined isolation thickness thereby allowing a minimal isolation distance of said copper conductor in a circuit that approaches said predetermined isolation thickness.

53. (Withdrawn) The method of claim 52, wherein said low permittivity insulating layer comprises Hydrogen Silsesquioxane (HSQ), said concentration of copper at which leakage current becomes significant is approximately 10^{19} atoms/cm^3 and said distance of copper diffusion at said concentration of approximately 10^{19} atoms/cm^3 is approximately 50 nm.

54. (Withdrawn) The method of claim 53, wherein said predetermined isolation thickness provides a separation distance between two copper conductors that approaches approximately 0.2 to 0.3 μm.

55. (Withdrawn) The method of claim 53, further comprising:

depositing an adhesion layer between said HSQ layer and said copper conductor.

56. (Withdrawn) The method of claim 55, wherein said adhesion layer comprises a material having an etching rate approximately equal to an etching rate of said copper conductor.

57. (Currently amended) A semiconductor device, comprising:

a first interlayer insulating layer;

a plurality of wiring lines which are formed of copper (CU), said plurality of wiring lines formed on said first interlayer insulating layer;

~~an~~ a second insulating layer which has a property that Cu ~~is unlikely to enter~~ diffuses into said second insulating layer at a concentration of approximately 10^{19} atoms/cm^3 in a first region adjacent to each said wiring line, said concentration decreasing in accordance with a diffusion gradient in a second region down to between 10^{18} atoms/cm^3 and 10^{19} atoms/cm^3 and a third region wherein said concentration is no greater than an order of magnitude of 10^{18} atoms/cm^3 and which said third region serves to insulates between said plurality of wiring lines; and

a second interlayer insulating layer formed on said second insulating layer ~~having the property that the Cu is unlikely to enter therein~~,

wherein ~~said insulating layer has surface regions whose Cu concentrations is equal to or higher than 10^{19} atoms/cm^3, and~~ a separation distance between at least two of said Cu wiring lines approaches a minimum ~~consistent with maintaining a separation between said surface regions~~ for said third region.

58. (Currently amended) A semiconductor device, comprising:

a plurality ~~fo~~ of copper (Cu) wiring lines; and

an insulating layer which insulates between said plurality of Cu wiring lines,

wherein said insulating layer has surface regions respectively adjacent to said wiring lines whose Cu concentration is equal to or higher than 10^{19} atoms/cm^3 due to a diffusion of Cu from said Cu wiring lines, and a separation distance between at least two of said Cu wiring lines is approximately 0.2 to 0.3 μm.